supplying an unlock signal generated on the basis of an unlock instruction to the cache memory to reset the replace-inhibition state of at least one of the cache blocks such that replacing said at least one of the cache blocks to the main memory is allowed.

19. (NEW) A method of controlling a cache memory connected to a main memory and divided into a plurality of cache blocks, comprising:

supplying a lock instruction to set a replace-inhibition state of at least one of the cache blocks in which replacing said at least one of the cache blocks to the main memory is inhibited;

supplying an unlock instruction to reset the replace inhibition state of at least one of the cache clocks such that replacing said at least one of the cache block to the main memory is allowed; and

performing either reading or writing of the main memory by using the remaining cache blocks of the cache memory, other than said at least one of the cache blocks, such that, when the replace-inhibition state is set by the lock instruction, replacing said at least one of the cache blocks to the main memory is inhibited during the reading or writing of the main memory.

20. (NEW) The computer according to claim 15 further comprising a cache controller controlling the cache memory, the cache controller comprising:

a first unit performing a switching to allow the cache memory to act as the random access memory;

a second unit setting a range of the cache memory in which the cache memory is acting as the random access memory;

a third unit setting an address space of the random access memory; and

a fourth unit receiving a notification from the cache memory when an address space of the cache memory acting as the random access memory is accessed, and accessing an external storage device when an address outside the address space of the cache memory is accessed.

REMARKS

I. STATUS OF THE CLAIMS

Claims 1-17 were previously pending.

Claims 14 and 16 are canceled, without prejudice or disclaimer.

New claims 18-20 are added.

In view of the above, it is submitted that claims 1-3, 15, and 17-20 are submitted for consideration herein.

II. OBJECTION TO THE TITLE

Page 2 of the Office Action states that the title of the invention is not descriptive and 'The title should be more specific to differentiate the invention from similar inventions in the patent literature. It appears that lock/unlock and cache acting as random access memory aspects of the invention should be mentioned in the title so that the title is more descriptive.'

The Applicant submits that the Title, "METHOD OF CONTROLLING A CACHE MEMORY TO INCREASE AN ACCESS SPEED TO A MAIN MEMORY, AND A COMPUTER USING THE METHOD" is sufficiently descriptive. There is no requirement in the MPEP that the title of an invention differentiate the invention from similar inventions. MPEP 606 states that the title should be brief. Nevertheless, if the Examiner wishes to suggest a new title he feels is appropriate, the Applicant may consider same.

III. REJECTION OF CLAIMS 1-12 UNDER 35 U.S.C. § 102

Page 3 of the Office Action rejects claims 1-12 under 35 U.S.C. § 102(e) as being anticipated by MacDonald, U.S. Patent No. 5,913,224 (Hereinafter "Macdonald").

Claim 1 (as amended) recites, "**supplying a lock**[/unlock] **signal generated on the basis of a lock instruction** to the cache memory to [either] set a replace-inhibition state of at least one of the cache blocks in which replacing said at least one of the cache blocks to the main memory is inhibited[, or reset the replace-inhibition state of at least one of the cache clocks such that replacing said at least one of the cache block to the main memory is allowed]; and performing either reading or writing of the main memory by using the remaining cache blocks of the cache memory, other than said at least one of the cache blocks, such that, **when the replace-inhibition state is set by the lock**[/unlock] signal, replacing said at least one of the cache blocks to the main memory is inhibited during the reading or writing of the main memory. "

(emphasis added).

In MacDonald, a computer system in which the lock bits of the cache memory are set to the lock state when the real time code is executed.

However, unlike MacDonald, the present invention recites **supplying a lock signal generated on the basis of a lock instruction** to the cache memory . . . replacing the cache blocks to the main memory is inhibited. MacDonald is limited to setting lock bits of cache memory, but does not disclose a lock instruction as claimed.

Further, the lock of MacDonald relates to only locking the cache itself, but not disclosing replacing at least one of the cache blocks to the main memory is inhibited during the reading or writing of the main memory. The lock of MacDonald applies only to the cache itself, but not does not inhibit the main memory.

Thus, the present invention typically increases a degree of freedom of lock bit handling.

Therefore, MacDonald does not anticipate claim 1.

Claim 7 recites, "**determining that an address designated by an instruction matches with an address of at least one of the cache blocks of the cache memory**; and

supplying, when a lock/unlock instruction is received from a CPU and the match is determined, a lock/unlock signal to the cache memory to either set a replace-inhibition state of said at least one of the cache blocks in which **replacing said at least one of the cache blocks to the main memory or the peripheral system is inhibited**, or reset the replace-inhibition state of said at least one of the cache blocks such that replacing said at least one of the cache blocks to the main memory or the peripheral system is allowed." (emphasis added)

As stated above, MacDonald does not disclose the lock instruction, as claimed. MacDonald serves to lock only bits in the cache itself, but does not inhibit replacing at least one of the cache blocks to the main memory of the peripheral system, as claimed. Note that the Abstract of MacDonald states, "Lock bits associated with each line of cache lock the contents of the lines preventing the line from being overwritten under normal cache operation in which the least most recently used cached data is replaced by presently accessed data." MacDonald replaces cache data with new cache data, but does not affect the main memory.

In view of the above, independent claims 4 and 8 is not anticipated by MacDonald.

Therefore, in view of the above, withdrawal of the rejections is respectfully requested.

IV. REJECTION OF CLAIMS 13-17 UNDER 35 U.S.C. § 102

Page 6 of the Office Action rejects claims 13-17 under 35 U.S.C. § 102(e) as being anticipated by Briggs, U.S. Patent No. 5,410,669.

Claim 13 (as amended) recites, "determining whether the cache memory is acting as the random access memory; and assigning a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory, wherein the computer includes a bus control unit **connecting the main memory and the cache memory, and a peripheral system connected to the computer through the bus control unit**, and wherein, when the cache memory is acting as the random access memory and an access request externally sent from an address outside the second address space of the cache memory is received, **the computer accesses one of the main memory or the peripheral system instead of the cache memory**." (emphasis added).

Briggs discloses a data processor having a bus interface controller 10. However, Briggs does not connect the main memory and the cache memory . . . and when the cache memory is acting as the random access memory and an access request externally sent from an address . . . is received, the computer accesses one of the main memory or the peripheral system instead of the cache memory. Briggs implements a cache memory but does not allow access of a main memory or a peripheral system instead of the cache memory.

Claim 15 (as amended) recites, "a determination unit which determines whether the cache memory is acting as the random access memory; [and] an assignment unit which assigns a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory; and

a selection unit which selects one of a first assignment state and a second assignment state for the cache memory in response to a control signal, wherein, when the first assignment state is selected by the selection unit, the second address space is assigned for the cache memory, and when the second assignment state is selected by the selection unit, a third address space that partially overlaps the first address space is assigned for the cache memory."

Briggs does not disclose a third address space that partially overlaps the first address space is assigned for the cache memory, when the second assignment state is selected for the cache memory. Briggs does not disclose such a third address space.

Claim 17 (as amended) recites, "a determination unit which determines whether the cache memory is acting as the random access memory; an assignment unit which assigns a

second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory; a bus control unit connecting the main memory and the cache memory; a peripheral system connected to the computer through the bus control unit; and an access control unit which accesses one of the main memory or the peripheral system instead of the cache memory when the cache memory is acting as the random access memory and an access request externally sent from an address outside the second address space of the cache memory is received. "

Biggs does not disclose the determination unit and the assignment unit, as claimed.

Therefore, in view of all of the above, withdrawal of the rejections is respectfully requested.

V. NEW CLAIMS 18-20

New claims 18-20 are added which recite features not taught or suggested by the applied art, as discussed above. Therefore, it is submitted that new claims 18-20 are in condition for allowance.

VI. CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 10/10/02

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CERTIFICATE UNDER 37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231

on 10/10, 20 02

STAAS & HALSEY

By: _____

Date: 10/10/02

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please CANCEL claims 14 and 16, without prejudice or disclaimer.

Please AMEND the following claims:

1. (ONCE AMENDED) A method of controlling a cache memory connected to a main memory and divided into a plurality of cache blocks, [which is executed by a computer that accesses the main memory through the cache memory,] comprising [the steps of]:

supplying a lock[/unlock] signal generated on the basis of a lock instruction to the cache memory to [either] set a replace-inhibition state of at least one of the cache blocks in which replacing said at least one of the cache blocks to the main memory is inhibited[, or reset the replace-inhibition state of at least one of the cache clocks such that replacing said at least one of the cache block to the main memory is allowed]; and

performing either reading or writing of the main memory by using the remaining cache blocks of the cache memory, other than said at least one of the cache blocks, such that, when the replace-inhibition state is set by the lock[/unlock] signal, replacing said at least one of the cache blocks to the main memory is inhibited during the reading or writing of the main memory.

2. (AS ORIGINAL) The method according to claim 1, wherein, in said supplying step, at least one of flags corresponding to the cache blocks is set when the replace-inhibition state is set by the lock/unlock signal, and said at least one of the flags is reset when the replace-inhibition state is reset by the lock/unlock signal, and in said performing step, replacing the cache blocks, the flags of which are set, to the main memory is inhibited during the reading or writing of the main memory.

3. (AS ORIGINAL) The method according to claim 1, wherein, when an all unlock instruction is supplied to the cache memory in said supplying step, all the replace-inhibition states of the cache blocks are reset by the all unlock instruction such that replacing all the cache blocks of the cache memory to the main memory is allowed.

4. (ONCE AMENDED) A computer including a main memory and a cache memory, the cache memory being connected to the main memory and divided into a plurality of cache blocks, comprising:

a block state setting unit which supplies a lock[/unlock] signal generated on the basis of a lock instruction to the cache memory to [either] set a replace-inhibition state of at least one of the cache blocks in which replacing said at least one of the cache blocks to the main memory is inhibited, [or reset the replace-inhibition state of at least one of the cache clocks such that replacing said at least one of the cache block to the main memory is allowed]; and

a reading/writing unit which performs either reading or writing of the main memory by using the remaining cache blocks of the cache memory, other than said at least one of the cache blocks, such that, when the replace-inhibition state is set by the lock[/unlock] signal supplied by the block state setting unit, replacing said at least one of the cache blocks to the main memory is inhibited during the reading or writing of the main memory.

5. (AS ORIGINAL) The computer according to claim 4, wherein the block state setting unit sets at least one of flags corresponding to the cache blocks when setting the replace-inhibition state by the lock/unlock signal, and resets at least one of the flags corresponding to the cache blocks when resetting the replace-inhibition state by the lock/unlock signal, and wherein the reading/writing unit inhibits writing the cache blocks, the flags of which are set by the block state setting unit, to the main memory during the reading or writing of the main memory.

6. (AS ORIGINAL) The computer according to claim 4, wherein the block state setting unit is configured to supply an all unlock instruction to the cache memory when resetting all the replace-inhibition states of the cache blocks, so that writing all the cache blocks of the cache memory to the main memory is allowed.

7. (ONCE AMENDED) A method of controlling a cache memory connected to a main memory and a peripheral system and divided into a plurality of cache blocks, comprising [the steps of]:

determining that an address designated by an instruction matches with an address of at least one of the cache blocks of the cache memory; and

supplying, when a lock/unlock instruction is received from a CPU and the match is

determined, a lock/unlock signal to the cache memory to either set a replace-inhibition state of said at least one of the cache blocks in which replacing said at least one of the cache blocks to the main memory or the peripheral system is inhibited, or reset the replace-inhibition state of said at least one of the cache blocks such that replacing said at least one of the cache blocks to the main memory or the peripheral system is allowed.

8. (AS ORIGINAL) A computer including a main memory and a cache memory, the cache memory being connected to the main memory and a peripheral system and divided into a plurality of cache blocks, comprising:

a comparator which determines that an address designated by an instruction matches with an address of at least one of the cache blocks; and

a lock/unlock control unit which supplies, when a lock/unlock instruction is received from a CPU and the match is determined by the comparator, a lock/unlock signal to the cache memory to either set a replace-inhibition state of said at least one of the cache blocks in which replacing said at least one of the cache blocks to the main memory or the peripheral system is inhibited, or reset the replace-inhibition state of said at least one of the cache blocks such that replacing said at least one of the cache blocks to the main memory or the peripheral system is allowed.

9. (AS ORIGINAL) The computer according to claim 8, further comprising a load control unit which supplies, when a load instruction is received from the CPU and the match is determined by the comparator, a load signal to the cache memory to load data of said at least one of the cache blocks to the CPU.

10. (AS ORIGINAL) The computer according to claim 8, further comprising a store control unit which supplies, when a store instruction is received from the CPU and the match is determined by the comparator, a store signal to the cache memory to store data from the CPU into said at least one of the cache blocks of the cache memory.

11. (AS ORIGINAL) The computer according to claim 8, further comprising a flash control unit which supplies, when a flash instruction is received from the CPU and the match is determined by the comparator, a flash signal to the cache memory to transfer data of said at least one of the cache blocks to the main memory or the peripheral system.

12. (AS ORIGINAL) The computer according to claim 8, further comprising an invalidate control unit which supplies, when an invalidate instruction is received from the CPU and the match is determined by the comparator, an invalidate signal to the cache memory to invalidate said at least one of the cache blocks of the cache memory.

13. (ONCE AMENDED) A method of controlling a cache memory that is connected to a main memory with a first address space and capable of acting as a random access memory, which is executed by a computer that accesses the main memory through the cache memory, comprising [the steps of]:

determining whether the cache memory is acting as the random access memory; and

assigning a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory,

wherein the computer includes a bus control unit connecting the main memory and the cache memory, and a peripheral system connected to the computer through the bus control unit, and

wherein, when the cache memory is acting as the random access memory and an access request externally sent from an address outside the second address space of the cache memory is received, the computer accesses one of the main memory or the peripheral system instead of the cache memory.

14. (CANCELED)

15. (ONCE AMENDED) A computer including a main memory and a cache memory, the main memory having a first address space and the cache memory being capable of acting as a random access memory, comprising:

a determination unit which determines whether the cache memory is acting as the random access memory; [and]

an assignment unit which assigns a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory; and

a selection unit which selects one of a first assignment state and a second assignment

state for the cache memory in response to a control signal, wherein, when the first assignment state is selected by the selection unit, the second address space is assigned for the cache memory, and when the second assignment state is selected by the selection unit, a third address space that partially overlaps the first address space is assigned for the cache memory.

16. (CANCELED)

17. (ONCE AMENDED) A computer including a main memory and a cache memory, the main memory having a first address space and the cache memory being capable of acting as a random access memory, [The computer according to claim 15, further] comprising:

a determination unit which determines whether the cache memory is acting as the random access memory;

an assignment unit which assigns a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory;

a bus control unit connecting the main memory and the cache memory;

a peripheral system connected to the computer through the bus control unit; and

an access control unit which accesses one of the main memory or the peripheral system instead of the cache memory when the cache memory is acting as the random access memory and an access request externally sent from an address outside the second address space of the cache memory is received.

Please ADD the following NEW claims 18-20:

18. (NEW) The method according to claim 1, further comprising the operation of supplying an unlock signal generated on the basis of an unlock instruction to the cache memory to reset the replace-inhibition state of at least one of the cache blocks such that replacing said at least one of the cache blocks to the main memory is allowed.

19. (NEW) A method of controlling a cache memory connected to a main memory and divided into a plurality of cache blocks, comprising:

supplying a lock instruction to set a replace-inhibition state of at least one of the cache blocks in which replacing said at least one of the cache blocks to the main memory is inhibited;

supplying an unlock instruction to reset the replace inhibition state of at least one of the cache clocks such that replacing said at least one of the cache block to the main memory is allowed; and

performing either reading or writing of the main memory by using the remaining cache blocks of the cache memory, other than said at least one of the cache blocks, such that, when the replace-inhibition state is set by the lock instruction, replacing said at least one of the cache blocks to the main memory is inhibited during the reading or writing of the main memory.

20. (NEW) The computer according to claim 15 further comprising a cache controller controlling the cache memory, the cache controller comprising:

a first unit performing a switching to allow the cache memory to act as the random access memory;

a second unit setting a range of the cache memory in which the cache memory is acting as the random access memory;

a third unit setting an address space of the random access memory; and

a fourth unit receiving a notification from the cache memory when an address space of the cache memory acting as the random access memory is accessed, and accessing an external storage device when an address outside the address space of the cache memory is accessed.